INTERLEAVED SWITCHING TOPOLOGY FOR THREE-PHASE POWER-FACTOR CORRECTION

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ABSTRACT

Single-switch boost stages, connected between three-phase rectifiers and DC-link capacitors, allow good power-factor correction when operated in the discontinuous-conduction-mode. This paper is presented to aid design at all operating levels of this converter type. For high output power, it is shown that reduced component stress and higher power-factor, results using interleaved switching topologies. Some experimental results from a laboratory model are presented.

INTRODUCTION

The single-switch three-phase boost converter shown in Fig. 1 gives good power-factor correction if the circuit is operated in the discontinuous conduction mode. Prasad (4), Simonetti (5) and Kolar (3) have shown such circuits give an economical and easily controlled method of realising single-quadrant low to medium power three-phase power supplies which comply with the strictest statutory line-frequency harmonic current limits.

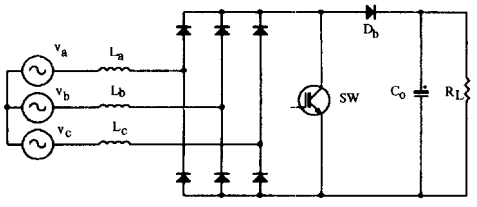

Figure 1: Single-switch three-phase Boost converter circuit.

To increase the power handling capability of systems, single-switch boost stages can be connected to operate in parallel, as shown in Fig 2. Moreover, it is beneficial to phase shift gating signals the stages by $360/s$ degrees; where s is the number of stages. The effect of using multiple, up to four, single-switch boost stages with such interleaved switching is to artificially raise input and output switching ripple frequency, reduce passive input and output volume and reduce switch (e.g. IGBT) peak current levels. Also the input current waveforms are improved significantly (compare Figs. 6 and 7).

An analysis of interleaved parallel-stage circuits now follows. The resulting performance and design data has largely been produced as a result of numerical solution of the normalised circuit equations, but the results have also been verified using SPICE circuit simulation and observations on practical circuits.

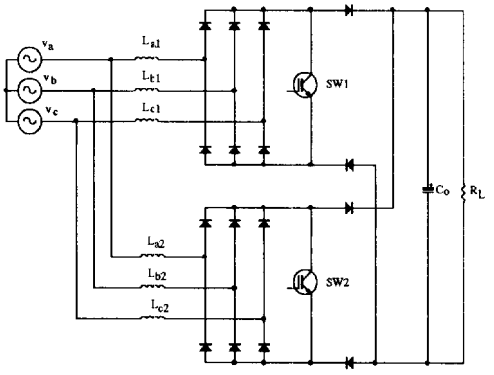

Figure 2: Parallel connection of two single-switch boost stage.

CIRCUIT ANALYSIS

During the analysis it will be assumed that the circuit is operated under the following conditions:

- the switching frequency is significantly higher than line frequency, ($f_{sw} >> f_o$), so that input voltage may be assumed constant during a switching period.
- constant output voltage V_o.
- all components are ideal and semiconductor device volt drops are negligible.
- three-phase voltage supply is balanced and purely sinusoidal, according to the following expressions:

$$\begin{aligned} v_a &= V_m \sin(\omega t) \\ v_b &= V_m \sin(\omega t - 2\pi/3) \\ v_c &= V_m \sin(\omega t - 4\pi/3) \end{aligned} \qquad (1)$$

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Voltage conversion ratio

The maximum line-to-line input voltage, say v_{ab}, occurs at $\omega t=\pi/3$, when v_c is zero. From this fact the peak input current may be determined. When the switch is on, the input circuit of Fig. 1 can be drawn as in Fig. 3(a). The inductor current i_{La} ramps up to i_{Lapeak} at the end of t_{on}, while i_{Lc} is zero and i_{Lb} is equal but opposite to i_{La}. The peak current is defined by

$$i_{Lpeak} = \frac{V_m}{L} \cdot \sin\left(\frac{\pi}{3}\right) \cdot D \cdot t_{sw} \qquad (2)$$

where $D = t_{on} / t_{sw}$ and $t_{sw} = 1/f_{sw}$

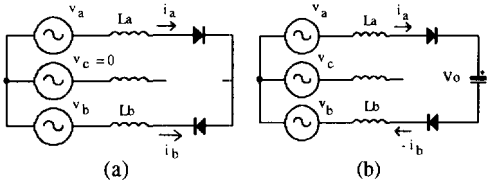


Figure 3: At $\omega t=\pi/3$; (a) switch *SW* is on. (b) switch *SW* is off.

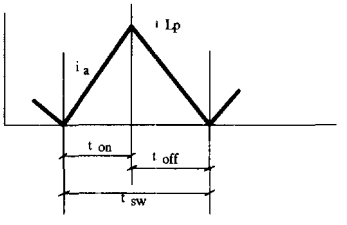


Figure 4: Inductor current of phase *a* at $\omega t=\pi/3$.

When the switch is off, circuit operation is presented by the equivalent circuit in Fig. 3(b). Diode D_b, (Fig. 1) is conducting and the output capacitor is charged. For line input currents to be discontinuous, inductor currents i_{La} and i_{Lb} have to reach zero at the end of t_{sw}. Using the Kirchhoff voltage law, the circuit equations become

$$v_a - v_b - 2L\frac{di_{La}}{dt} - V_o = 0 \qquad (3)$$

Under this condition, the current falls to zero right at the end of the switching period, not before. Hence $t_{on}+t_{off}$ must equal t_{sw}.

$$\frac{di_{La}}{dt} \approx \frac{\Delta i_{La}}{\Delta t} \quad \text{and}$$
$$\Delta i_{La} = i_{Lpeak}; \qquad \Delta t = t_{off} = (1-D) \cdot t_{sw}$$

Substituting Δi_{La} and Δt into Equation 3 and equating i_{Lpeak} with Equation 2, gives the voltage conversion ratio.

$$\frac{V_o}{V_m} = \sqrt{3} \cdot a \qquad ; \qquad a = \frac{1}{1-D} \qquad (4)$$

The output voltage V_o used here is the minimum value. Which this will ensures that the line input currents are always discontinuous.

Line input current analysis

When switch *SW*, (Fig. 1) is turned on. The diode D_b is reversed biased and forced off. The three inductors are then connected as a three-phase balanced star load, and their currents change according to their phase voltages and turn-on time. The inductor currents and output voltage are obtained using the following state equations:

$$L\frac{di_{Lk}}{dt} = v_k \qquad \text{where} \quad k = a,b,c \qquad (5)$$

$$C_o\frac{dv_o}{dt} = -\frac{V_o}{R_L} \qquad (6)$$

The inductor currents start from zero and their peak-values at the end of turn on time, t_{on} is

$$i_{Lkpeak} = \frac{v_k}{L} \cdot D \cdot t_{sw} \qquad (7)$$

When the switch *SW* is turned off, the inductor currents freewheel through the boost diode, D_b, and the load cell $C_d R_L$. Circuit state-equations become

$$L\frac{di_{Lk}}{dt} = v_k + \alpha_k \cdot v_o \qquad \text{where } k = a,b,c \qquad (8)$$

$$C_o\frac{dv_o}{dt} = i_r - \frac{V_o}{R_L} \qquad (9)$$

α_k is a coefficient which depends on the value of phase angle ωt. Values are given in the Appendix. i_r is the free-wheeling current which flows through D_b.

The slope of the inductor currents reverses and the inductor current falls to zero. Equation (8) and (9) are valid when none of the inductor currents is zero, (see, t_{1r} in Fig. 5). The smallest current vanishes at the end of t_{1r}. Then the remaining inductor fall at a new rate and reach zero together the end of t_{2r}. They remain zero until the next switching period.

There are twelve $\pi/6$ sub-intervals in any line-frequency period. The reset times and rate of change of the remaining two inductor currents after the lowest current vanished can be found. For example, during the interval $0 \le \omega t < \pi/6$, i_{La} reaches zero first, and the

normalised reset times t_{1rn} t_{2rn} and di_{Lb}/dt di_{Lc}/dt can be defined as:

$$t_{1rn} = -\frac{\sin \omega t}{\sin(\omega t - a/\sqrt{3})} \tag{10}$$

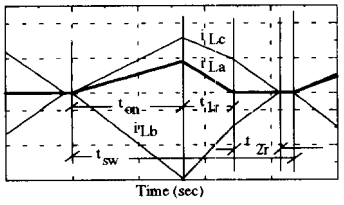


Figure 5: Inductor current waveforms over a switching period; where $0<\omega t<\pi/6$.

$$t_{2rn} = -\frac{\left[\sin\left(\omega t - \frac{2\pi}{3}\right) + t_{1rn}\left\{\sin\left(\omega t - \frac{2\pi}{3}\right) + \frac{2}{\sqrt{3}}a\right\}\right]}{\frac{\sqrt{3}}{2}\left[a + \sin\left(\omega t - \frac{\pi}{3}\right)\right]} \tag{11}$$

The normalised time is $t_{rn} = \frac{t_r}{D \cdot t_{sw}}$

$$\frac{di_{Lb}}{dt} = \frac{1}{2L}\left[(v_b - v_c) + v_o\right] \tag{12}$$

$$\frac{di_{Lc}}{dt} = -\frac{1}{2L}\left[(v_b - v_c) + v_o\right] \tag{13}$$

The output voltage becomes

$$C_o \frac{dv_o}{dt} = -i_{Lb} - \frac{V_o}{R_L} \tag{14}$$

The numerical solution of the state equation from the previous analysis gives the normalised input-line current waveform and its spectrum shown in Fig. 6.

Normalised current $i_{Ln} = \frac{i_L}{i_{Lpeak}}$

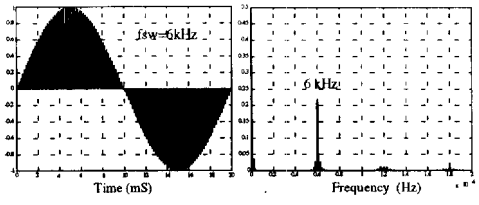


Figure 6: (a) Input-line current waveform ; i_{LI}, and (b) its spectrum, at switching frequency f_{sw}.= 6 kHz.

From the line-current spectrum, it can be seen that there is a high switching frequency related content and content at the 5th and 7th line-frequency harmonics. The amplitudes are (f_{sw}) 50%, (5th) 7% and (7th) 1.3% of the fundamental frequency component. The variation in 5th and 7th with D is shown in more detail in Fig. 11.

INTERLEAVED SWITCHING

The parallel connection of stages, e.g. as shown in Fig. 2, improves the input current waveform significantly when switching is interleaved. Fig. 7 gives an input current waveform and its spectrum when the switching frequency is half that in Fig. 6. From the spectra in Fig. 7(b), it is evident that the result is better than doubling the f_{sw} of a single stage.

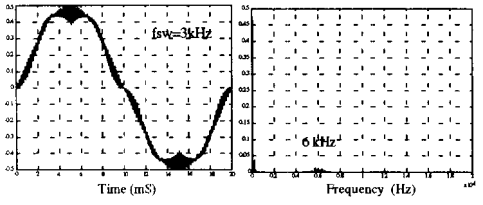


Figure 7: current waveform and frequency spectrum of two interleaved stages operated at f_{sw} = 3 kHz.

The power-factor of the un-filtered circuit is considerably improved, namely $0.953< p.f.<0.996$ for $0.2<D>0.5$ as shown in Fig. 10.

For interleaved parallel circuits minimised input filter L-C components are required, since the high frequency harmonics are small. Moreover, L-C product is inversely proportional to f_r^2, which can be seen from a line-input filter equivalent circuit in Fig. 8 and Equation 15. Where I_{ifr} and I_{Ifr} are ripple frequency components at the converter and the main line input, respectively.

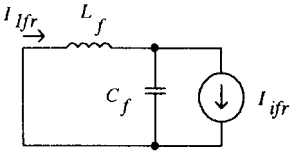


Figure 8: Per phase equivalent circuit for filter design.

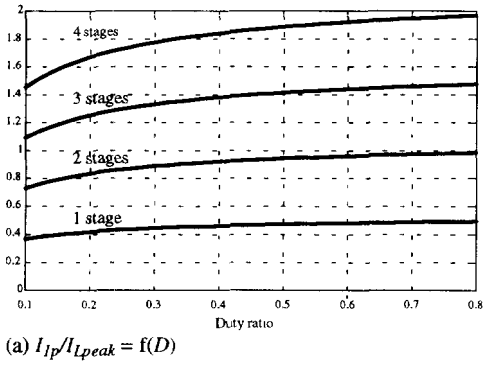
$$L_f C_f = \frac{1}{(2\pi f_r)^2}\left[1 + \frac{I_{ifr}}{I_{1fr}}\right] \tag{15}$$

Boost-circuit line-inductance volume does not significantly alter, despite twice as many inductors being required, because the peak-current is halved and

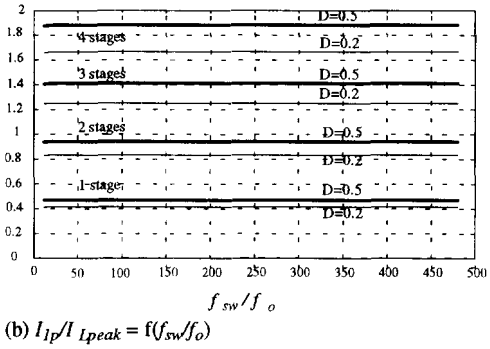
the inductor value is doubled giving no net change in stored energy.

DESIGN DATA

The design and operation of single or multi-stages boost converters may be investigated from the following graphs. All of these have been produced using Equations 1-14.



(a) I_{lp}/I_{Lpeak} = f(D)



(b) I_{lp}/I_{Lpeak} = f(f_{sw}/f_o)

Figure 9: Graph of I_{lp}/I_{Lpeak} versus duty- ratio and f_{sw}/f_o.

The relationship between the fundamental component and the peak value of inductor current against duty-ratio and f_{sw}/f_o are shown in Fig 9 (a) and (b). Over a wide f_{sw}/f_o range, the ratio of line-frequency current fundamental to peak-current at any duty-ratio is approximately constant, as shown in Fig. 9 (b). This simplifies the determination of boost-circuit inductor value. Similarly, graphs in Fig 12 (a)-(c) show normalised value of rectifier diode, boost-switch and boost-diode current for one stage to aid the choice of component current ratings.

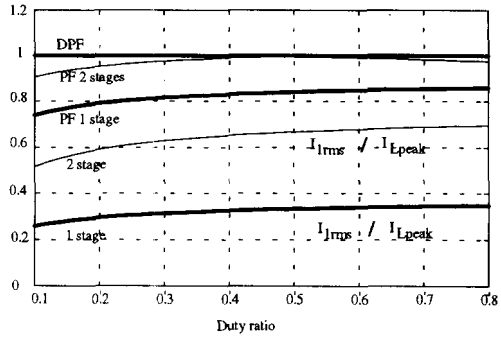


Figure 10: Power-factor and I_{1rms}/I_{Lpeak} versus duty-ratio.

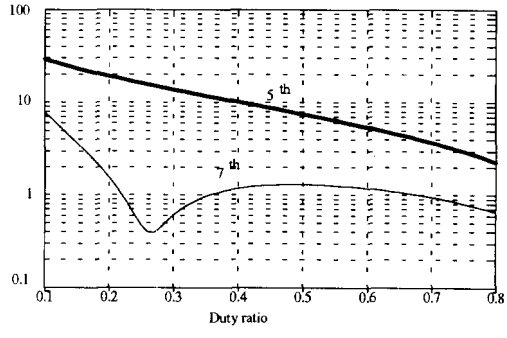


Figure 11: Amplitude of 5^{th} and 7^{th} line current harmonics for one stage and 2 stages relative to the fundamental component of line current.

Although high order harmonics are very small in multi-stage converters, low order harmonics still remain a problem, especially the 5^{th} and 7^{th} harmonics as shown in Fig 11.

CIRCUIT DESIGN EXAMPLE

Both single and multi-stage circuit with interleaving can be designed, using the design data in the following procedure.

1. Determine the worst-case duty ratio of the circuit using the minimum DC output voltage , the minimum supply voltage and maximum output power.

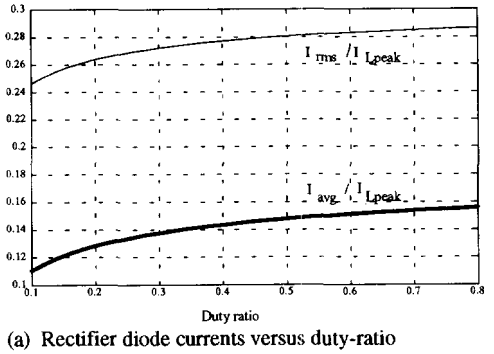
2. Calculate the peak of fundamental line-input current.

3. From the graph in Fig. 9, at the specific D, read a number off the y-axis for the desired stage. This

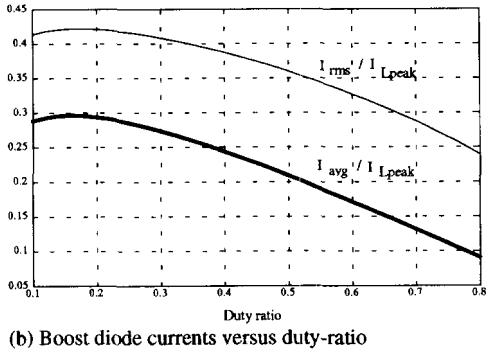
is the relation between the peak fundamental line-input current and inductor peak current, I_{1p}/I_{Lpeak}.

4. Calculate the boost inductor from

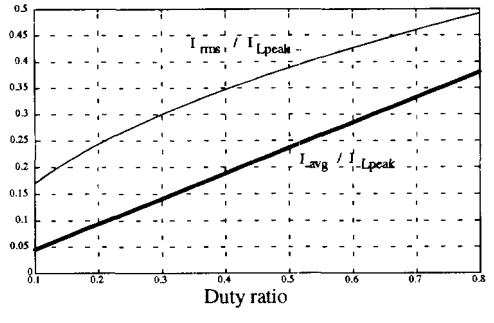
$$L_{\max} = \frac{V_m}{I_{Lpeak}} \cdot D \cdot t_{sw} \qquad (16)$$



(a) Rectifier diode currents versus duty-ratio



(b) Boost diode currents versus duty-ratio



(c) Switch currents for all stages versus duty-ratio

Figure 12: I_{rms}/I_{Lpeak} and I_{avg}/I_{Lpeak}= f(D) of bridge rectifier diode, boost diode and boost switch.

Example

Design a single-stage three-phase single-switch boost converter for operating at

Phase voltage:	50	Volts
Line-frequency:	50	Hz
Maximum output power:	500	Watts
DC output voltage:	245	Volts
Switching frequency:	20	kHz

1. Using $V_o = \frac{1}{(1-D)}\sqrt{3}V_m$

gives a duty ratio of $D = 0.5$

2. Assuming 100% conversion efficiency, i.e.

$P_i = P_o$= 500 W

$$I_{1rms} = \frac{P_i}{3V_s} = \frac{500}{3 \cdot 50}$$

I_{1rms} = 3.3333 A; I_{1peak} = 4.714 A.

3. From graph in Fig. 9, for 1 stage and D=0.5,

$$\frac{I_{1peak}}{I_{Lpeak}} = 0.47 \quad \text{therefore } I_{Lpeak} = 10.029 \text{ A.}$$

4. Equation 16, gives the maximum inductance

L_{max} = 176.26 μH

The calculated inductance L_{max} value may also be used in an interleaved two-stage converter design which gives the same output voltage. However the maximum output power is then doubled, i.e. 1000 W.

EXPERIMENT RESULT

The designed 1000 W two-stage converter, shown in Fig. 2, has been built and examined experimentally. Due to the source inductance, L_s, of the three-phase auto-transformer, three capacitors are added at the input-end of the boost inductors to reduce the effect of L_s, and form a line input filter.

A line-current waveform at phase a without line input filter and its phase voltage are shown in Fig. 13. It can be seen that the current is in phase but quite heavy distorted because low order harmonic content mainly the 5^{th} and 7^{th} still remain (Fig 14); approximately 9 % and 1.5 % of the fundamental current, respectively. However, the high frequency content is very small. By using the discontinuous conduction mode of operation, low-order harmonics cannot be totally eliminated from the converter input current. A further reduction is possible by neutralising harmonic currents with a small additional converter as shown in Fig.15.

The harmonic neutralising converter can be any type of active power filter, e.g. voltage source active power filter circuit.

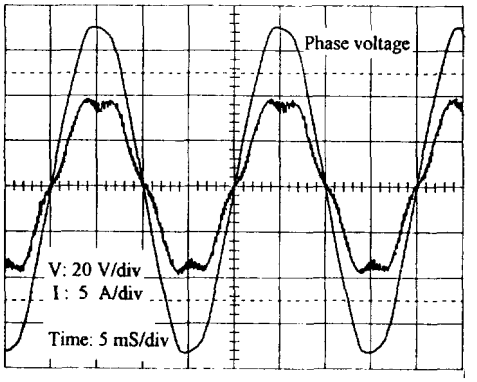


Figure 13: Phase voltage and input current.

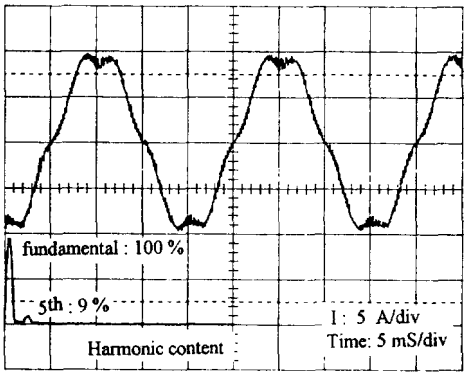


Figure 14: Input current and frequency content.

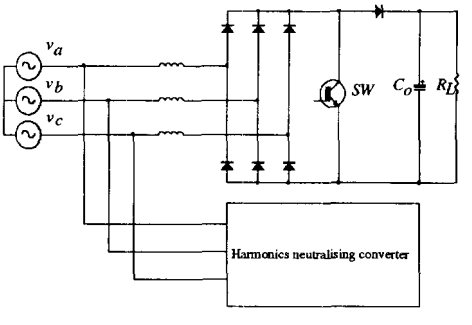


Figure 15: A three-phase power converter with a harmonic neutralising circuit.

CONCLUSION

Some design graphs are produced to aid the design of the three-phase single-switch boost converter. To improve line input currents, reduce the L-C input filter, output capacitor volume and reduce the current stress of switching devices, an interleaved switching topology is presented. This three-phase interleaving technique can be applied to other three-phase single-switch converters which have similar circuit characteristics, such as, SEPIC and CUK topologies.

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APPENDIX

Table 1 Coefficient for using in equation (8).

	ωt					
	0-π/3	π/3-2π/3	2π/3-π	π-4π/3	4π/3-5π/3	5π/3-2π
α_a	-1/3	-2/3	-1/3	1/3	2/3	1/3
α_b	2/3	1/3	-1/3	-2/3	-1/3	1/3
α_c	-1/3	1/3	2/3	1/3	-1/3	-2/3
i_r	$-i_{Lb}$	i_{La}	$i_{La}+i_{Lb}$	i_{Lb}	$-i_{La}$	$-i_{La}-i_{Lb}$